Analog Power Filters

V_3.3 — V_3.3_USB — FB2 600Ohm — V_USB_AVDD — C112 1uF — C102 1uF — C113 100nF — C103 100nF — C104 10uF

V_1.8 — V_1.8_DC_DC — FB3 600Ohm — FB4 600Ohm — V_SRD_AVDD — C120 1uF — C110 1uF — C111 10uF — C121 10uF

V_CMN18 — FB5 600Ohm — V_CMN18_AVDD — C122 1uF — C123 1uF — C124 100nF — C125 100nF — C126 100nF — C127 10uF — C128 10uF

V_1.0 — V_IHB_10 — FB6 600Ohm — V_AP_MCI_AVDD — C135 1uF — C136 1uF — C137 100nF — C138 10uF

V_CPA_VDD — C139 10uF — C140 10uF — C141 10uF

V_CPA_VDD — C144 100nF — C145 100nF — C581 100nF — C582 100nF

V_1.2 — V_DDR — FB7 600Ohm — V_CP1_MCI_AVDD — C146 1uF — C147 1uF — C148 100nF — C149 100nF — C150 10uF

V_VDDO_A — C152 100nF — C142 100nF

V_VDDO_B — C154 100nF — C158 10uF

V_VDDO_H — C151 100nF — C143 100nF

V_VDDO_C

V_VDDO_D

V_3.3 — V_VDDO_E — V_CP_VDDO_CMN — C173 100nF — C174 10uF

V_VDDO_A — V_VDDO_B — V_VDDO_C — V_VDDO_D — V_VDDO_E — V_VDDO_H

V_1.8 — V_2.5 — V_3.3 — R436 0 — R437 0 Assy = DNP — V_2.5_LDO

V_SDRAM_MV — C176 100nF — C179 100nF — C180 100nF — C181 100nF — C182 100nF — C183 100nF — C184 100nF — C185 100nF — C186 100nF — C578 100nF — C187 10uF — C188 10uF

V_1.8 — FB8 600Ohm — V_PLL_AVDD — C198 1uF — C200 1uF — C199 100nF

U1E

V_CPA_VDD	N25 CP0_VDD[0]	AP_VDD[0] K14	V_AP_VDD
	P22 CP0_VDD[1]	AP_VDD[1] K16	
	P26 CP0_VDD[2]	AP_VDD[2] L13	
	R23 CP0_VDD[3]	AP_VDD[3] L15	
	R27 CP0_VDD[4]	AP_VDD[4] L19	
	T24 CP0_VDD[5]	AP_VDD[5] M16	
	U25 CP0_VDD[6]	AP_VDD[6] M20	
	V22 CP0_VDD[7]	AP_VDD[7] N13	
	V26 CP0_VDD[8]	AP_VDD[8] N17	
	W23 CP0_VDD[9]	AP_VDD[9] P14	
	W27 CP0_VDD[10]	AP_VDD[10] P18	
	Y24 CP0_VDD[11]	AP_VDD[11] R15	
	Y28 CP0_VDD[12]	AP_VDD[12] R19	
		AP_VDD[13] T16	
		AP_VDD[14] T20	
		AP_VDD[15] U13	
		AP_VDD[16] U17	
		AP_VDD[17] U21	
		AP_VDD[18] V14	
		AP_VDD[19] V18	
		AP_VDD[20] W15	
		AP_VDD[21] W19	
		AP_VDD[22] Y16	
		AP_VDD[23] Y20	
		AP_VDD[24] AA13	
		AP_VDD[25] AA17	
		AP_VDD[26] AB18	
		AP_VDD[27]	
TP3 Assy = DNP — CP0_AVS_FB	F34 CP0_AVS_FB	AP_AVS_FB	AL21 AP_AVS_FB
	V_CP0_VDD		
	AC23 CP1_VDD[0]		
	AC27 CP1_VDD[1]		
	AD24 CP1_VDD[2]		
	AE21 CP1_VDD[3]		
	AE25 CP1_VDD[4]		
	AF22 CP1_VDD[5]		
	AF26 CP1_VDD[6]		
	AG23 CP1_VDD[7]		
	AH24 CP1_VDD[8]		
	AJ21 CP1_VDD[9]		
	AJ25 CP1_VDD[10]		
	AK22 CP1_VDD[11]		
	AK26 CP1_VDD[12]		
TP4 Assy = DNP — CP1_AVS_FB	W37 CP1_AVS_FB		
	V_VDDO_A		
	AK28 CP1_VDDO_A[0]	AP_VDDO_H[0] AA15	V_VDDO_H
	AK30 CP1_VDDO_A[1]	AP_VDDO_H[1] AB16	
	V_VDDO_B	AP_VDDO_H[2] AC15	
	AL25 CP1_VDDO_B[0]	AP_VDDO_M[0] K12	V_SDRAM_MV
	AL27 CP1_VDDO_B[1]	AP_VDDO_M[1] L11	
	AM26 CP1_VDDO_B[2]	AP_VDDO_M[2] M12	
	AM28 CP1_VDDO_B[3]	AP_VDDO_M[3] N11	
	V_VDDO_C	AP_VDDO_M[4] P12	
	L27 CP0_VDDO_C[0]	AP_VDDO_M[5] R11	
	M26 CP0_VDDO_C[1]	AP_VDDO_M[6] T12	
	V_VDDO_D	AP_VDDO_M[7] U11	
	L25 CP0_VDDO_D[0]	AP_VDDO_M[8] V12	
	M24 CP0_VDDO_D[1]	AP_VDDO_M[9] W11	
	V_VDDO_E	AP_VDDO_M[10] Y12	
	L23 CP0_VDDO_E[0]	AP_VDDO_M[11] AA11	
	M22 CP0_VDDO_E[1]	AP_VDDO_M[12] AB12	
	V_CMN18_AVDD	AP_VDDO_M[13] AB14	
	AA21 CMN_AVDD[0]	AP_VDDO_M[14] AC13	
	AA23 CMN_AVDD[1]	AP_VDDO_M[15] AC15	
	AB20 CMN_AVDD[2]	AP_PLL_AVDD N21	V_PLL_AVDD
	AC17 CMN_AVDD[3]		
	AC23 CMN_AVDD[4]	AP_MCI_AVDD AA19	V_AP_MCI_AVDD
	AM22 CP1_MCI_AVDD[0]		
	AM24 CP1_MCI_AVDD[1]		
	V_SRD_AVDD		
	N29 CP_SRD_AVDD[0]	CP_VDDO_CMN[0] AB22	V_CP_VDDO_CMN
	P28 CP_SRD_AVDD[1]	CP_VDDO_CMN[1] AB24	
	R29 CP_SRD_AVDD[2]	CP_VDDO_CMN[2] AB26	
	T28 CP_SRD_AVDD[3]		
	U29 CP_SRD_AVDD[4]		
	W29 CP_SRD_AVDD[5]		
	AA29 CP_SRD_AVDD[6]	AP_VHV AC21	AP_VHV
	AB28 CP_SRD_AVDD[7]		
	AC29 CP_SRD_AVDD[8]		
	AD28 CP_SRD_AVDD[9]		
	AE29 CP_SRD_AVDD[10]		
	AF28 CP_SRD_AVDD[11]		
	AG29 CP_SRD_AVDD[12]		
	AH28 CP_SRD_AVDD[13]		
	V_USB_AVDD		
	V30 CP0_USB_AVDD		
	V_3.3		
	L29 CP0_VDDO_JTAG[0]		
	M28 CP0_VDDO_JTAG[1]		
	V_3.3		
	L21 CP0_LDO_AVDD		
LDOA_CTRL — V_2.5_LDO	LDOA_CTRL_R F20 CP0_LDO_CTRL		
	LDOA_SENSE_R H20 CP0_LDO_SENSE		
	V_USB_AVDD AJ29 CP1_USB_AVDD		
C170 100nF	V_RTC AL29 CP1_RTC_AVDD		
	CP0_VHV N23 CP0_VHV		
	CP1_VHV AA25 CP1_VHV		

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V_AP_VDD — C95 100nF — C96 100nF — C97 100nF — C98 100nF — C99 100nF — C100 100nF — C101 100nF — C578 100nF

V_AP_VDD — C105 100nF — C114 10uF — C115 10uF — C116 10uF — C117 10uF

V_AP_VDD — C106 100nF — C118 100nF — C103 100nF — C108 100nF — C119 100nF — C109 100nF

V_SRD_AVDD — C120 100nF — C130 100nF — C131 100nF — C132 100nF — C133 100nF — C134 100nF

U1F

A1	VSS[0]	VSS[100]	N9
A33	VSS[1]	VSS[101]	N15
A35	VSS[2]	VSS[102]	N19
A39	VSS[3]	VSS[103]	N27
A41	VSS[4]	VSS[104]	N31
B18	VSS[5]	VSS[105]	N33
B38	VSS[6]	VSS[106]	N35
C33	VSS[7]	VSS[107]	N37
C35	VSS[8]	VSS[108]	N41
C41	VSS[9]	VSS[109]	P4
D4	VSS[10]	VSS[110]	P6
D6	VSS[11]	VSS[111]	P8
D8	VSS[12]	VSS[112]	P10
D10	VSS[13]	VSS[113]	P16
D12	VSS[14]	VSS[114]	P20
D14	VSS[15]	VSS[115]	P24
D16	VSS[16]	VSS[116]	P30
D18	VSS[17]	VSS[117]	P32
D38	VSS[18]	VSS[118]	P36
E19	VSS[19]	VSS[119]	P38
E21	VSS[20]	VSS[120]	P40
E23	VSS[21]	VSS[121]	R9
E25	VSS[22]	VSS[122]	R13
E27	VSS[23]	VSS[123]	R17
E29	VSS[24]	VSS[124]	R21
E31	VSS[25]	VSS[125]	R25
E33	VSS[26]	VSS[126]	R31
E37	VSS[27]	VSS[127]	R35
E41	VSS[28]	VSS[128]	R39
F4	VSS[29]	VSS[129]	R41
F6	VSS[30]	VSS[130]	T4
F8	VSS[31]	VSS[131]	T6
F10	VSS[32]	VSS[132]	T8
F12	VSS[33]	VSS[133]	T10
F14	VSS[34]	VSS[134]	T14
F16	VSS[35]	VSS[135]	T18
F18	VSS[36]	VSS[136]	T22
F38	VSS[37]	VSS[137]	T26
G19	VSS[38]	VSS[138]	T30
G21	VSS[39]	VSS[139]	T32
G23	VSS[40]	VSS[140]	T34
G25	VSS[41]	VSS[141]	T38
G27	VSS[42]	VSS[142]	U9
G29	VSS[43]	VSS[143]	U15
G31	VSS[44]	VSS[144]	U19
G33	VSS[45]	VSS[145]	U23
G35	VSS[46]	VSS[146]	U27
G41	VSS[47]	VSS[147]	U31
H4	VSS[48]	VSS[148]	U33
H6	VSS[49]	VSS[149]	U35
H8	VSS[50]	VSS[150]	U37
H10	VSS[51]	VSS[151]	V4
H12	VSS[52]	VSS[152]	V6
H14	VSS[53]	VSS[153]	V8
H16	VSS[54]	VSS[154]	V10
H18	VSS[55]	VSS[155]	V16
H38	VSS[56]	VSS[156]	V20
J11	VSS[57]	VSS[157]	V24
J13	VSS[58]	VSS[158]	V28
J15	VSS[59]	VSS[159]	V32
J17	VSS[60]	VSS[160]	V36
J19	VSS[61]	VSS[161]	V38
J21	VSS[62]	VSS[162]	W9
J23	VSS[63]	VSS[163]	W13
J25	VSS[64]	VSS[164]	W17
J27	VSS[65]	VSS[165]	W21
J29	VSS[66]	VSS[166]	W25
J31	VSS[67]	VSS[167]	W31
J33	VSS[68]	VSS[168]	W35
J35	VSS[69]	VSS[169]	W39
J37	VSS[70]	VSS[170]	W41
J41	VSS[71]	VSS[171]	Y4
K4	VSS[72]	VSS[172]	Y6
K6	VSS[73]	VSS[173]	Y8
K8	VSS[74]	VSS[174]	Y10
K10	VSS[75]	VSS[175]	Y14
K20	VSS[76]	VSS[176]	Y18
K22	VSS[77]	VSS[177]	Y22
K24	VSS[78]	VSS[178]	Y26
K26	VSS[79]	VSS[179]	Y30
K28	VSS[80]	VSS[180]	Y32
K30	VSS[81]	VSS[181]	Y34
K32	VSS[82]	VSS[182]	Y38
K36	VSS[83]	VSS[183]	AA9
K38	VSS[84]	VSS[184]	AA27
L9	VSS[85]	VSS[185]	AA31
L17	VSS[86]	VSS[186]	AA33
L31	VSS[87]	VSS[187]	AA35
L41	VSS[88]	VSS[188]	AA37
M4	VSS[89]	VSS[189]	AB4
M6	VSS[90]	VSS[190]	AB6
M8	VSS[91]	VSS[191]	AB8
M10	VSS[92]	VSS[192]	AB10
M14	VSS[93]	VSS[193]	AB30
M18	VSS[94]	VSS[194]	AB32
M30	VSS[95]	VSS[195]	AB34
M32	VSS[96]	VSS[196]	AB36
M34	VSS[97]	VSS[197]	AB38
M36	VSS[98]	VSS[198]	AC9
M38	VSS[99]	VSS[199]	AC19
			AC25

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U1G

AC31	VSS[200]	VSS[284]	AM20
AC35	VSS[201]	VSS[285]	AM32
AC39	VSS[202]	VSS[286]	AM36
AC41	VSS[203]	VSS[287]	AM38
AD4	VSS[204]	VSS[288]	AN6
AD6	VSS[205]	VSS[289]	AN10
AD8	VSS[206]	VSS[290]	AN14
AD10	VSS[207]	VSS[291]	AN18
AD12	VSS[208]	VSS[292]	AN22
AD14	VSS[209]	VSS[293]	AN26
AD16	VSS[210]	VSS[294]	AN30
AD18	VSS[211]	VSS[295]	AN34
AD20	VSS[212]	VSS[296]	AN38
AD22	VSS[213]	VSS[297]	AN42
AD26	VSS[214]	VSS[298]	AP2
AD30	VSS[215]	VSS[299]	AP6
AD32	VSS[216]	VSS[300]	AP10
AD36	VSS[217]	VSS[301]	AP14
AD38	VSS[218]	VSS[302]	AP18
AE9	VSS[219]	VSS[303]	AP22
AE11	VSS[220]	VSS[304]	AP26
AE23	VSS[221]	VSS[305]	AP30
AE27	VSS[222]	VSS[306]	AP34
AE31	VSS[223]	VSS[307]	AP38
AE33	VSS[224]	VSS[308]	AP42
AE35	VSS[225]	VSS[309]	AR4
AE37	VSS[226]	VSS[310]	AR8
AE41	VSS[227]	VSS[311]	AR12
AF4	VSS[228]	VSS[312]	AR16
AF6	VSS[229]	VSS[313]	AR20
AF8	VSS[230]	VSS[314]	AR24
AF10	VSS[231]	VSS[315]	AR28
AF24	VSS[232]	VSS[316]	AR32
AF30	VSS[233]	VSS[317]	AR36
AF32	VSS[234]	VSS[318]	AR40
AF34	VSS[235]	VSS[319]	AT2
AF38	VSS[236]	VSS[320]	AT6
AG9	VSS[237]	VSS[321]	AT10
AG11	VSS[238]	VSS[322]	AT14
AG21	VSS[239]	VSS[323]	AT18
AG25	VSS[240]	VSS[324]	AT22
AG27	VSS[241]	VSS[325]	AT26
AG31	VSS[242]	VSS[326]	AT30
AG35	VSS[243]	VSS[327]	AT34
AG41	VSS[244]	VSS[328]	AT38
AH4	VSS[245]	VSS[329]	AT42
AH6	VSS[246]	VSS[330]	AU1
AH8	VSS[247]	VSS[331]	AU5
AH10	VSS[248]	VSS[332]	AU9
AH22	VSS[249]	VSS[333]	AU13
AH26	VSS[250]	VSS[334]	AU17
AH30	VSS[251]	VSS[335]	AU21
AH32	VSS[252]	VSS[336]	AU25
AH34	VSS[253]	VSS[337]	AU29
AH38	VSS[254]	VSS[338]	AU33
AJ9	VSS[255]	VSS[339]	AU37
AJ11	VSS[256]	VSS[340]	AU41
AJ23	VSS[257]	VSS[341]	AV2
AJ27	VSS[258]	VSS[342]	AV6
AJ31	VSS[259]	VSS[343]	AV10
AJ35	VSS[260]	VSS[344]	AV14
AJ37	VSS[261]	VSS[345]	AV18
AJ41	VSS[262]	VSS[346]	AV22
AK4	VSS[263]	VSS[347]	AV26
AK6	VSS[264]	VSS[348]	AV30
AK8	VSS[265]	VSS[349]	AV34
AK10	VSS[266]	VSS[350]	AV38
AK24	VSS[267]	VSS[351]	AV42
AK32	VSS[268]	VSS[352]	AW1
AK34	VSS[269]	VSS[353]	AW5
AK38	VSS[270]	VSS[354]	AW9
AL9	VSS[271]	VSS[355]	AW13
AL11	VSS[272]	VSS[356]	AW17
AL31	VSS[273]	VSS[357]	AW21
AL35	VSS[274]	VSS[358]	AW25
AL37	VSS[275]	VSS[359]	AW29
AL41	VSS[276]	VSS[360]	AW33
AM4	VSS[277]	VSS[361]	AW37
AM6	VSS[278]	VSS[362]	AW41
AM8	VSS[279]	VSS[363]	BA1
AM10	VSS[280]	VSS[364]	BA5
AM12	VSS[281]		BA9
AM16	VSS[282]	AP_RSVD_VSS	AL15
AM18	VSS[283]		

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R40 0

VHV Circuit

V_CPB_VDD — CP1_VHV — V_1.8

V_AP_VDD — AP_VHV — V_1.8

V_CPA_VDD — CP0_VHV — V_1.8

Place close to 7040 ! (0.5" to 0.7")

V_2.5_LDO (LDOA_SENSE) — V_3.3 — = Stlk: = LDO_A — LDO Test Jumper — LDOA_CTRL

V_CPB_VDD — C191 100nF — C192 100nF — C193 100nF — C194 100nF — C195 10uF — C196 10uF — C197 10uF

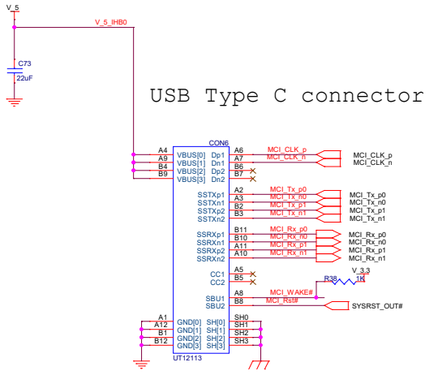
V_SDRAM_MV — C176 100nF — C179 100nF — C180 100nF — C181 100nF — C182 100nF — C183 100nF — C184 100nF — C185 100nF — C186 100nF — C578 100nF — C187 10uF — C188 10uF

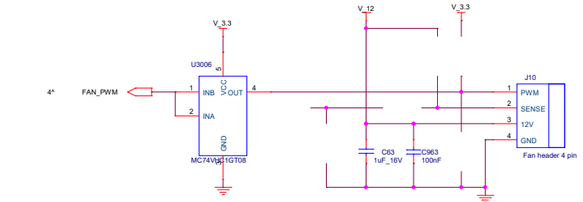
V_BAT_IN — V_3.3 — 1K — R41 — D1 BAT54C — V_RTC

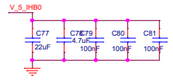
V_BAT_IN — J4 Header TH 50mil Assy = DNP — BT2 3002 Assy = DNP — BT1 SCR1620VE01S

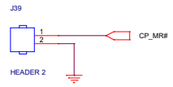
V_3.3 — C960 100nF — C959 100nF — C961 100nF — C962 100nF

USB Type C connector



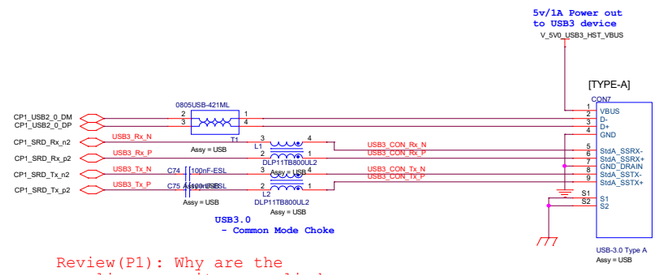






USB2.0 - Common Mode Choke

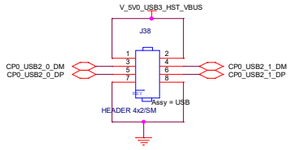
Connector side

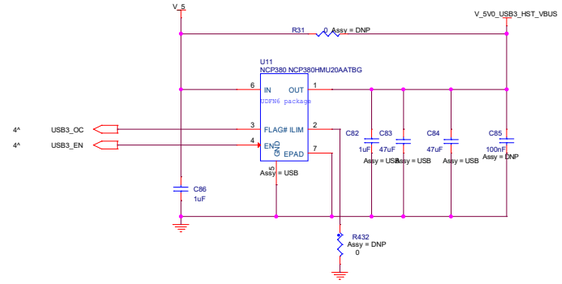


USB3.0 - Common Mode Choke

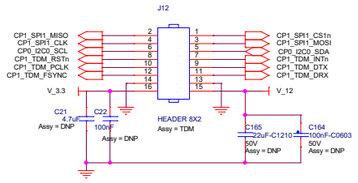
MV USB3.0 HOST

Review(P1): Why are the coupling capacitors applied to Tx path and not Rx.

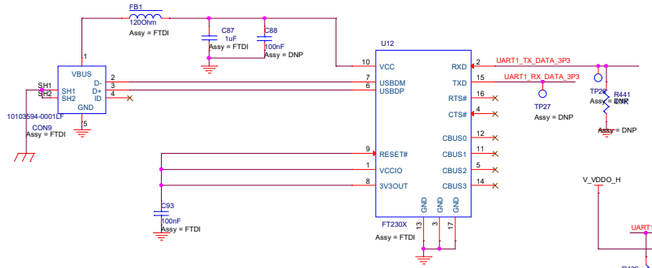


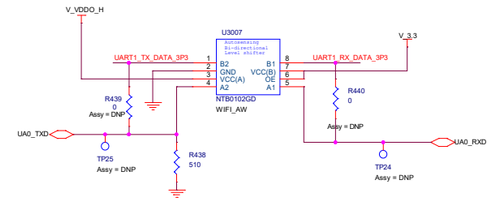


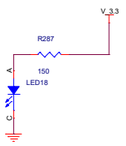
SLIC TDM Module connectors

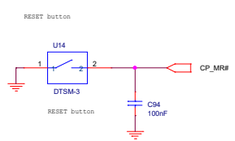


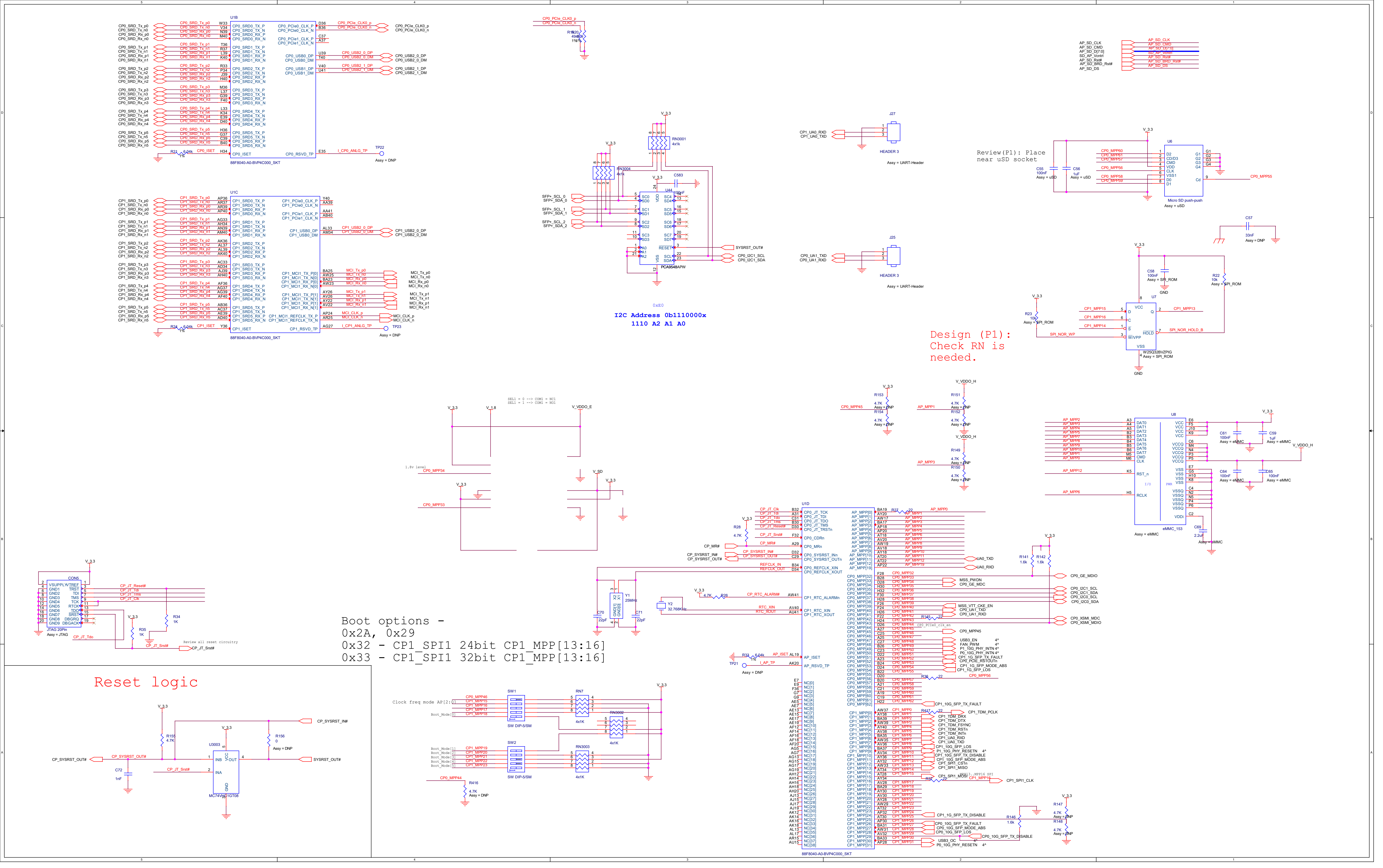
microUSB to UART











U1B
88F8040-A0-BVP4C000_SKT
U1C
U1D
I2C Address 0b1110000x
1110 A2 A1 A0
PCA9548APW
HEADER 3
Assy = UART-Header
Review(P1): Place
near uSD socket
Micro SD push-push
Design (P1):
Check RN is
needed.
W25Q32BVZPIG
eMMC_153
JTAG 20Pin
Boot options -
0x2A, 0x29
0x32 - CP1_SPI1 24bit CP1_MPP[13:16]
0x33 - CP1_SPI1 32bit CP1_MPP[13:16]
Reset logic
MC74VHC1GT08
SW DIP-5/SM

DDR Module Connectors

Review(P1): VPP and VREFCA must be on during self refresh

Review(P1): VPP must be active before V_DDR

To 88F6820 DDR power

Place near add/con. via's

DDR3

DDR4

M_NCAL[0]499 49̄9
M_PCAL[0]499 49̄9
M_NCAL[1]499 2ī5
M_PCAL[1]499 1ī50
M_NCAL[2]499 49̄9
M_PCAL[2]499 49̄9
M_NCAL[3]499 2ī5
M_PCAL[3]499 1ī50

Step Down DC/DC
Vin=5v, Vout=1.20v
DC current: 5A
Peak current: 7.5A

V_DCJACK_IN
CON10 KLDHCX-0202-A-LT
L12 90Ohm
L3 90Ohm
V_12
C201 10uF-C1210
C202 10uF-C1210
C203 10uF-C1210
L4 90Ohm
L13 90Ohm
C205 470pF 50V
C207 470pF 50V
J40 HEADER 2

Review the sentence from the design guide -
For any AVS operation, REF_CLK_25 must be toggling on board.
Review well
STAGE1_PG
U15 TPS53355
C209 1uF 25V 20% X5R
C212 22uF-C1210
C210 22uF-C1210
R50 82.5K
R51 187K
C213 1uF
R54 100K
R55 100K Assy = DNP
PGOOD
V_3.3
R44 4.7K
R45 1K Assy = DNP
C204 1nF
R48 2.2
C206 100nF
R49 4.7K
L5 0.33uH
C208 100nF
R52 3
C222 1.5nF
R42 10k
R43 4.99K
R46 0
AP_AVS_FB
R47 301
V_AP_VDD_SHNT
V_AP_VDD
R524 0.01 ohm
R523 0.01 ohm
R522 0.01 ohm
R521 0.01 ohm
C214 47uF
C217 47uF
C223 47uF
C226 47uF
C227 47uF
C228 47uF
C230 47uF
C232 47uF
C237 47uF
C238 47uF

V_5
U16 RT8073
C215 10uF
C211 10uF
GND
STAGE1_PG
PGOOD
EN
COMP
RT
SS
GND (E-Pad)
VIN1 VIN2
BOOT
LX1 LX2 LX3
FB
C216 100nF
L6 0.33uH
C218 10uF
C219 22uF Assy = DNP
C220 22uF
C221 22uF
PHY_0.8V
R53 0
R56 15.0K
R57 28.7K
C224 680pF 50V
C225 0.01UF 6.3V
R58 24.0K 1%

V_3.3_ATX
V_3.3
CON11 4200S-212TW2-L ATX CON
+3.3V[3] +3.3V[0] 1
-12V +3.3V[1] 2
GND[3] GND[0] 3
PS-ON +5V[0] 4
GND[4] GND[1] 5
GND[5] +5V[1] 6
GND[6] GND[2] 7
-5V PG 8
+5V[2] +5VSB 9
+5V[3] +12V[0] 10
+5V[4] +12V[1] 11
GND[7] +3.3V[2] 12
= Silk: o
= Silk: = 5VSB_ATX On
R431 PCB Short Assy = DNP
ATX_PS_ONn
V_5VSB_ATX
ATX_PWR_OK
C233 22uF
C234 22uF
C235 22uF Assy = DNP

V_12
U19 RT7290
C241 10uF-C0805
VIN
EN
LDO
VBYP
ENLDO
CLK
BOOT
SW SW SW SW
VOUT
PGND
AGND
PGOOD
VCC
C242 100nF
L7 1.5uH
C246 22uF
C247 22uF
C248 22uF
C249 22uF
C254 2.2uF Assy = DNP
Connect ENLDO and VBYP
R62 4.7K
C261 1uF

V_3.3
U17 MIC5317
VIN OUT
EN
GND NC
C239 1uF
C240 1uF

V_6
U18 AP7361C
C243 10uF
C244 10uF
GND
STAGE1_PG
PGOOD
EN
COMP
RT
SS
GND (E-Pad)
VIN1 VIN2
BOOT
LX1 LX2 LX3
FB
C245 100nF
L8 0.33uH
C250 10uF
C251 22uF Assy = DNP
C252 22uF
C253 22uF
V_CPB_VDD
V_CPA_VDD
R60 12K 1%
R64 24.0K 1%
R61 15.0K
R63 28.7K
C260 680pF 50V
C259 0.01UF 6.3V
RT8073

V_3.3
U21 AP7361C
IN OUT
GND
C255 10uF
C256 10uF
V_2.5
PHY_AVDD25

V_3.3
U20 NCP1117
IN OUT
GND EPD
C257 10uF Assy = DNP
C258 10uF
R435 0.005
PHY_AVDD20
V_1.8

V_5
U24 RT8073
C266 10uF
C267 10uF
GND
STAGE1_PG
PGOOD
EN
COMP
RT
SS
GND (E-Pad)
VIN1 VIN2
BOOT
LX1 LX2 LX3
FB
C268 100nF
L9 0.33uH
C269 10uF
C270 22uF Assy = DNP
C271 22uF
C272 22uF
V_DDR_SHNT
V_DDR
R434 0.01 ohm
R65 12K 1%
R69 24.0K 1%
R66 15.0K
R67 28.7K
C279 680pF 50V
C280 0.01UF 6.3V

V_12
U25 RT7291
C273 10uF-C0805
VIN
EN
LDO
VBYP
ENLDO
CLK
BOOT
SW SW SW SW
VOUT
PGND
AGND
PGOOD
VCC
C274 100nF
L10 1.5uH
V_5
C275 22uF
C276 22uF
C277 22uF
C278 22uF
C284 2.2uF Assy = DNP
Connect ENLDO and VBYP
STAGE1_PG
C286 1uF

V_3.3
U22 NCP1117
IN OUT
GND
C262 10uF
C263 10uF
PHY_P0_1.5V

V_3.3
U23 NCP1117
IN OUT
GND
C264 10uF
C265 10uF
PHY_P1_1.5V

V_5
U18 AP7361C
C290 10uF
C291 10uF
GND
STAGE1_PG
PGOOD
EN
COMP
RT
SS
GND (E-Pad)
VIN1 VIN2
BOOT
LX1 LX2 LX3
FB
C292 100nF
L11 0.47uH
C294 10uF
C295 22uF Assy = DNP
C296 22uF
C297 22uF
V_1.8_DC_DC
V_1.8
R74 30K 1%
R77 24.0K 1%
R75 15.0K
R76 28.7K
C299 680pF 50V
C300 0.01UF 6.3V
RT8073

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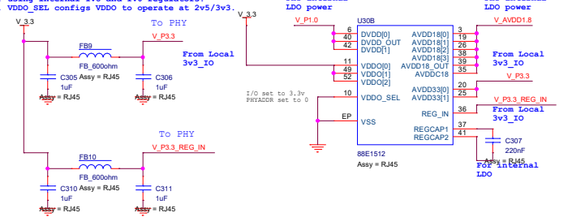
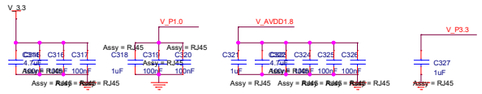
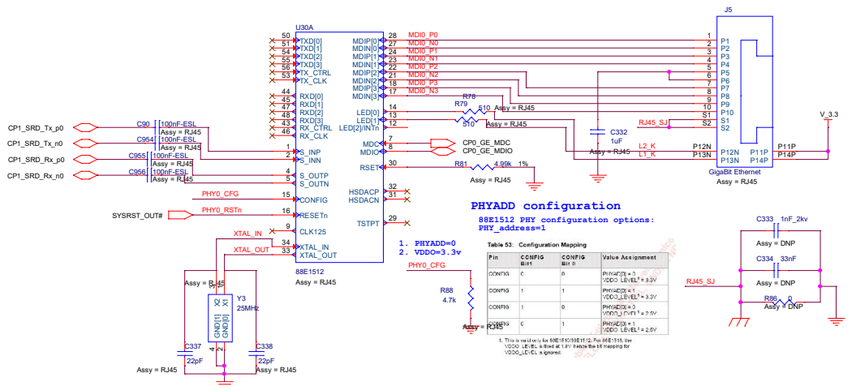
Date: Tuesday, November 01, 2016	Sheet 5 of 7	

PHY Power configurations

88E1512 power configurations:
1. using internal 1v8 and 1v0 regulators.
2. VDDO_SEL configs VDDO to operate at 2v5/3v3.







PHYADD configuration

88E1512 PHY configuration options:
PHY_address=1

1. PHYADD=0
2. VDDO=3.3v

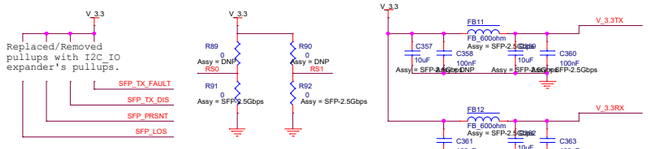
Table 53: Configuration Mapping

Pin	CONFIG Bit1	CONFIG Bit 0	Value Assignment
CONFIG	0	0	PHYADD[2:0] = 1 VDDO_LEVEL* = 3.3V
CONFIG	1	1	PHYADD[2:0] = 1 VDDO_LEVEL* = 3.3V
CONFIG	1	0	PHYADD[2:0] = 3 VDDO_LEVEL* = 2.5V
CONFIG	0	1	PHYADD[2:0] = 1 VDDO_LEVEL* = 2.5V

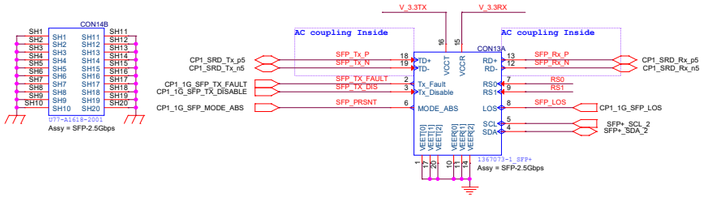
1. This is valid only for 88E1510/88E1512. For 88E1518, the VDDO_LEVEL is fixed at 1.8V. Therefore the bit mapping for VDDO_LEVEL is ignored.

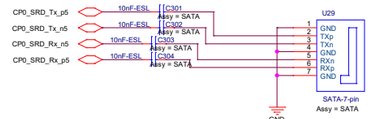
SFP + defines maximum current withdraw from V_3.3TX and V_3.3RX as 300mA each.

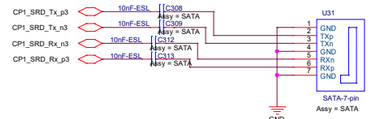
SFP TRANSCEIVER Power

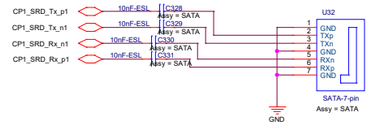


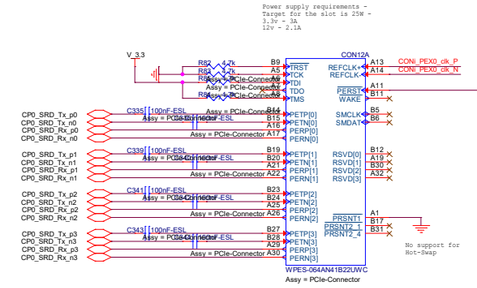
SFP TRANSCEIVER

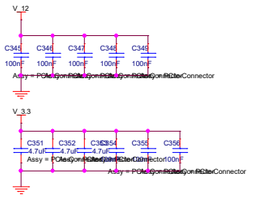


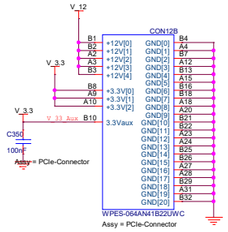












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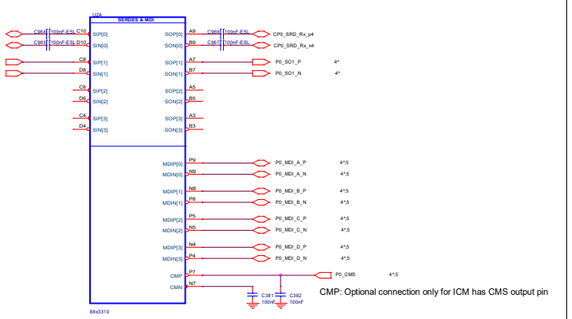
Date: Monday, October 31, 2016	Sheet 6 of 7	

CP0 10G 88x3310

Review(P1): Do we need dc unbiasing caps on SERDES lines?



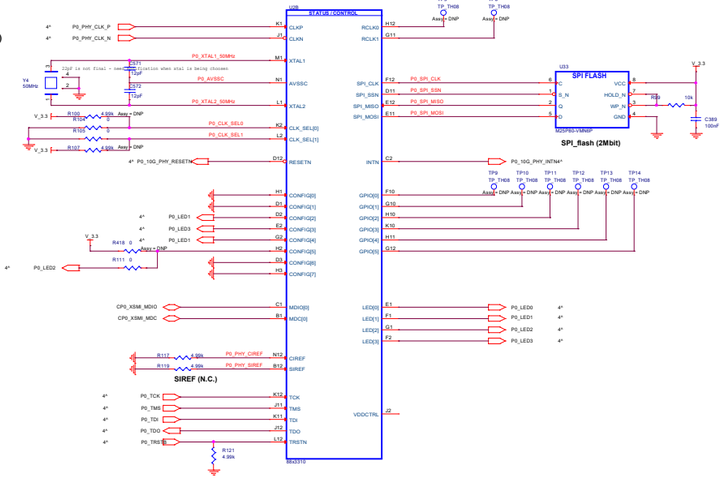
CLK_SEL[1:0]	Clock Input Selection
0 0	50MHz XTAL
0 1	50MHz CLK P/N
1 0	156.25MHz CLK P/N
1 1	Reserved

Pin	Bit 2	Bit 1	Bit 0
CONFIG[0]	PHYAD[4]	PHYAD[3]	PHYAD[2]
CONFIG[1]	ANEG_MS	PHYAD[1]	PHYAD[0]
CONFIG[2]	ANEG_SPD[2]	ANEG_SPD[1]	ANEG_SPD[0]
CONFIG[3]	MAC_TYPE[2]	MAC_TYPE[1]	MAC_TYPE[0]
CONFIG[4]	HOST_TYPE[2]	HOST_TYPE[1]	HOST_TYPE[0]
CONFIG[5]	SPI_CONFIG	FIBER_TYPE[1]	FIBER_TYPE[0]
CONFIG[6]	PHYAD[8]	F29[1]	F29[0]
CONFIG[7]	FACTORY_TEST	RESERVED	RESERVED

CMP: Optional connection only for ICM has CMS output pin

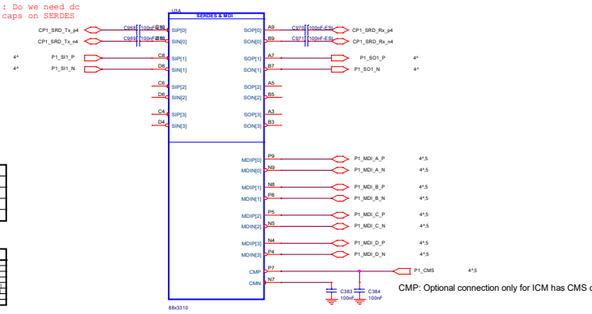
156.25MHz (LVPECL)

50MHz XTAL



CP1 10G 88x3310

Review(P1): Do we need dc unbiasing caps on SERDES lines?



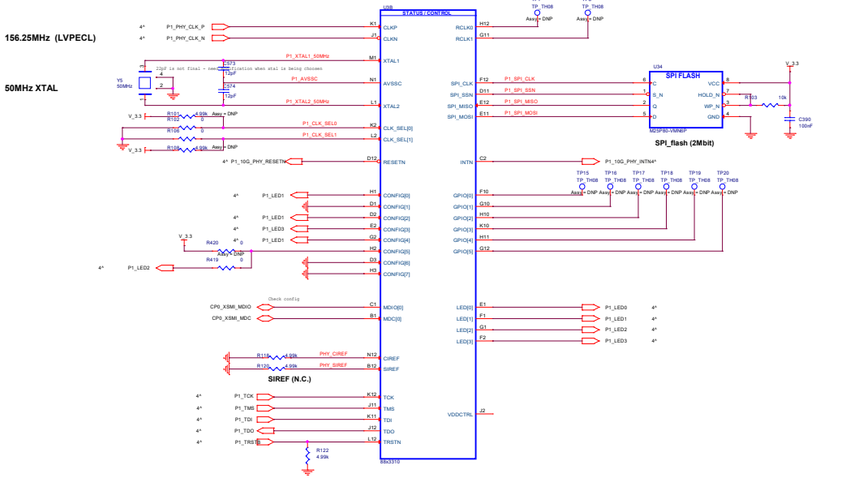
CLK_SEL[1:0]	Clock Input Selection
0 0	50MHz XTAL
0 1	50MHz CLK P/N
1 0	156.25MHz CLK P/N
1 1	Reserved

Pin	Bit 2	Bit 1	Bit 0
CONFIG[0]	PHYAD[4]	PHYAD[3]	PHYAD[2]
CONFIG[1]	ANEG_MS	PHYAD[1]	PHYAD[0]
CONFIG[2]	ANEG_SPD[2]	ANEG_SPD[1]	ANEG_SPD[0]
CONFIG[3]	MAC_TYPE[2]	MAC_TYPE[1]	MAC_TYPE[0]
CONFIG[4]	HOST_TYPE[2]	HOST_TYPE[1]	HOST_TYPE[0]
CONFIG[5]	SPI_CONFIG	FIBER_TYPE[1]	FIBER_TYPE[0]
CONFIG[6]	PHYAD[8]	F29[1]	F29[0]
CONFIG[7]	FACTORY_TEST	RESERVED	RESERVED

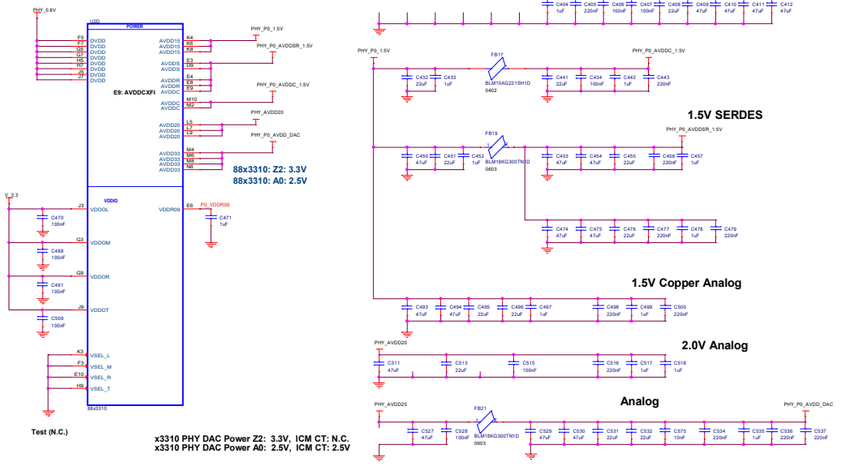
CMP: Optional connection only for ICM has CMS output pin

156.25MHz (LVPECL)

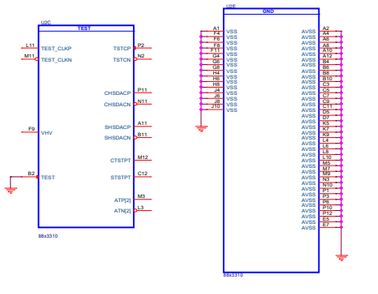
50MHz XTAL



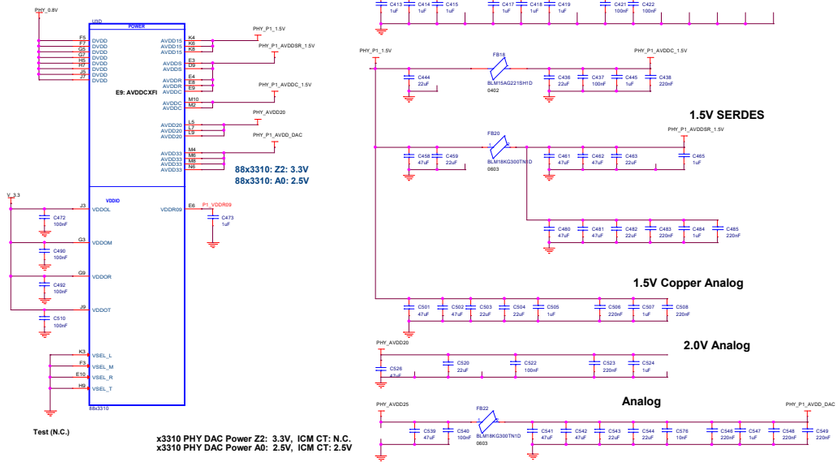
x3310 Hierarchy: Power and GND



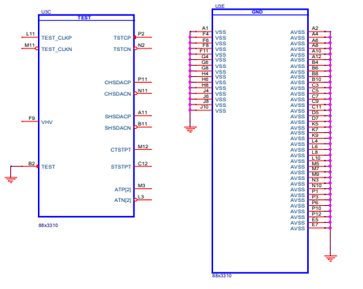
x3310 PHY DAC Power Z2: 3.3V, ICM CT: N.C.
x3310 PHY DAC Power A0: 2.5V, ICM CT: 2.5V



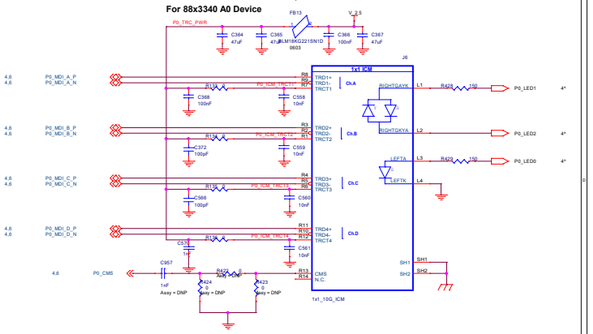
x3310 Hierarchy: Power and GND



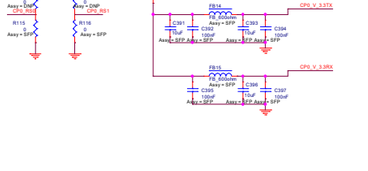
x3310 PHY DAC Power Z2: 3.3V, ICM CT: N.C.
x3310 PHY DAC Power A0: 2.5V, ICM CT: 2.5V



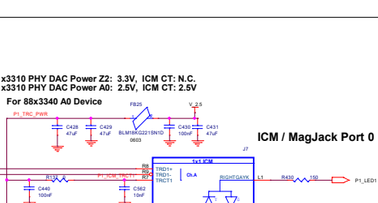
x3310 PHY DAC Power Z2: 3.3V, ICM CT: N.C.
x3310 PHY DAC Power A0: 2.5V, ICM CT: 2.5V
For 88x3340 A0 Device



Connect LEDs

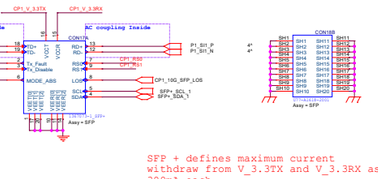


SFP + defines maximum current withdraw from V_3.3TX and V_3.3RX as 300mA each.

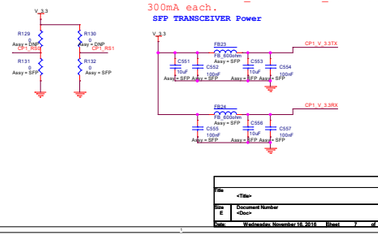


x3310 PHY DAC Power Z2: 3.3V, ICM CT: N.C.
x3310 PHY DAC Power A0: 2.5V, ICM CT: 2.5V
For 88x3340 A0 Device
ICM / MagJack Port 0

Connect LEDs



SFP + defines maximum current withdraw from V_3.3TX and V_3.3RX as 300mA each.



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